

CLAIMS

What is claimed is:

1. A method of high frequency operation in an integrated circuit, said
5 method comprising:
accessing charge stored in a capacitor comprising a plurality of deep
n well regions formed in an epitaxy region of said integrated circuit; and
coupling said charge to a transistor device of said integrated circuit
enabling switching at said high frequency.
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2. The method of Claim 1 wherein said capacitor further comprises
bulk p + material.
3. The method of Claim 1 wherein said capacitor further comprises a p
15 well.
4. The method of Claim 1 wherein said coupling is parasitic.
5. The method of Claim 1 wherein said plurality of deep n well regions
20 comprise substantially parallel stripes.
6. The method of Claim 1 wherein said plurality of deep n well regions
comprise a grid.

7. The method of Claim 1 wherein said plurality of deep n well regions comprise more than one layer of deep n well.

8. An integrated circuit comprising:

5 a plurality of transistors having a principal operating voltage;
a deep n well comprising n- material, wherein a portion of said deep n well is coupled to p type material which is coupled to a ground reference of said integrated circuit; and
wherein said deep n well is coupled to said principal operating
10 voltage of said plurality of transistors of said integrated circuit.

9. The integrated circuit of Claim 8 wherein said deep n well is substantially surrounded by p type material.

15 10. The integrated circuit of Claim 8 comprising a plurality of said deep n wells.

11. The integrated circuit of Claim 8 wherein said deep n well is parasitically coupled to said principal operating voltage.

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12. The integrated circuit of Claim 8 wherein said p type material comprises epitaxy.

13. The integrated circuit of Claim 8 wherein said p type material
25 comprises bulk p material.

14. The integrated circuit of Claim 8 wherein said p type material comprises a p well.

5 15. The integrated circuit of Claim 14 wherein said p well is at substantially a same depth as said deep n well.

16. An integrated circuit comprising:
a first deep n well at a first depth; and
10 a second deep n well at a second depth.

17. The integrated circuit of Claim 16 wherein said first and said second deep n wells are coupled together.

15 18. The integrated circuit of Claim 16 further comprising a plurality of transistors having a principal operating voltage and wherein said first and said second deep n wells are coupled to said principal operating voltage of said plurality of transistors of said integrated circuit.

20 19. The integrated circuit of Claim 16 wherein said first and said second deep n wells are coupled to a ground reference for said integrated circuit.

20. The integrated circuit of Claim 16 wherein said first and said second deep n wells are substantially surrounded by p type material.

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21. The integrated circuit of Claim 16 wherein said first and said second deep n wells are formed with the same process mask.

22. The integrated circuit of Claim 16 wherein said first and said second
5 deep n wells from a power supply decoupling capacitor.

23. The integrated circuit of Claim 16 comprising a p well at substantially said first depth.

10 24. An integrated circuit as described in Claim 16 further comprising a deep p well disposed between said first and said second deep n wells.

25. A deep n well capacitor comprising a deep n well region of an integrated circuit, said deep n well coupled to Vdd and ground.

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26. The deep n well capacitor of Claim 25 further comprising a plurality of deep n well regions coupled together.

27. The deep n well capacitor of Claim 26 wherein said plurality of deep
20 n well regions are substantially parallel.

28. The deep n well capacitor of Claim 26 wherein said plurality of deep n well regions comprise deep n well regions at different depths of said integrated circuit.

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29. The deep n well capacitor of Claim 26 comprising a plurality of p well regions at substantially the same depth as said plurality of deep n well regions and wherein said plurality of p well regions are disposed between said plurality of deep n well regions.

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30. The deep n well capacitor of Claim 25 wherein said deep n well region is substantially surrounded by p type material.

31. The deep n well capacitor of Claim 25 wherein said deep n well region
10 is parasitically coupled to said Vdd.